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09/749,731	12/28/2000	Katsuhiko Hara	35.C15028	6793

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EXAMINER	
PENDERGRASS, KYLE M	

ART UNIT	PAPER NUMBER
2624	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/749,731	HARA, KATSUHIKO	
	Examiner	Art Unit	
	Kyle M Pendergrass	2624	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 10/02.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

Claim 2 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In claim 2 the applicant improperly describes that the second bus is connected to the coding/decoding unit.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5 & 7-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Toujima et al. (US Patent No. 5,999,654) & Date et al. (European Patent No. 0,893,766).

Regarding claim 1, Toujima et al., discloses an image processing apparatus comprising: a first bus (Fig 4, bus 63) which is connected to a coding/decoding unit (Fig 4, encoder 51) of image data; a second bus (Fig 4, bus 62) which is connected to an image memory (Fig 4, DRAM 21) for storing the image data and used for transferring the image data; a control unit (Fig 4, encoding unit 50) for executing a coding process of said image data in accordance with a predetermined program (column 2, lines 31-36);

and switching control means (Fig 4, bus switch 60) for arbitrating connecting requests from the control/coding unit to said image memory and switching the connections of the buses, thereby enabling the image data to be coded by using said first bus during transfer of the image data using said second bus in accordance with a control by control unit (see column 2, lines 37-44). However, although Toujima et al., disclose a third bus 61, they do not disclose the third bus to be connected to the processing unit (encoding unit 50) that executes the coding process, which is disclosed by Toujima et al., to be connected to the first bus 63.

Date et al., discloses a third bus (Fig 4, P BUS) connected to a processing unit (Fig 4, CPU 401) in an image processing apparatus. Date et al., also discloses a switching control means (Fig 4, system bus bridge 402) that provides interconnection among the I/O bus (input/output), P bus (CPU) and MC bus (memory).

Accordingly, it would have been obvious to one skilled in the art to have used the switching control means and the additional bus connection that connects the processing unit as disclosed by Date et al., in the image transfer means of Toujima et al., because it was proven at the time of the invention to process a large quantity of data (Date et al. abstract), such as the image data used in the apparatus disclosed by Toujima et al. The capabilities of establishing two simultaneous system connections, as disclosed by Date et al., (page 14 lines 15-16) would let the Toujima et al., apparatus realize high-speed data transfer with a high degree of parallel operation which increases the functionality of the apparatus disclosed by Toujima et al.

Claim 8 recites identical features as claim 1 except claim 8 is a method claim. Thus, arguments similar to that presented above for claim 1 are equally applicable to claim 8.

Regarding claim 2, the rejection of claim 1 is representative of claim 2. See Date et al., disclosure of establishing two simultaneous system connections (page 7 lines 11-12 & page 14 lines 15-16). The system bus bridge is designed in such a manner that two pairs of buses can be connected in parallel. When combined with the Toujima et al., apparatus, the image data is coded by the coding/decoding unit by using the first bus in parallel with the image data transfer using the second bus.

Claim 9 recites identical features as claim 2 except claim 9 is a method claim. Thus, arguments similar to that presented above for claim 2 are equally applicable to claim 9.

Regarding claim 3, the rejection of claim 1 is representative of claim 3. See Date et al., disclosure of switching control means further comprising memory control means (Fig 4, memory controller 403), connected to the memory (MC) bus, for controlling said image memory; and bus control means (Fig 4, system bus bridge 402) which is connected to the CPU bus and further connected to said memory control means through a fourth bus (Fig 4, MC Bus). See Toujima et al., disclosure of bus control means (Fig 4, bus switch 60) connected to bus 63 of encoder 51.

Claim 10 recites identical features as claim 3 except claim 10 is a method claim. Thus, arguments similar to that presented above for claim 3 are equally applicable to claim 10.

Regarding claim 4, the claim rejection of claim 3 is representative of claim 4. See Date et al., disclosure of an image interface means (Fig 20, IO bus interface 2906) for connecting an image input apparatus or image output apparatus and transmitting and receiving the image data to/from the connected apparatus; and transfer control means for controlling the image data transfer between said image memory and said apparatus connected to said image interface means through said switching control means (see page 14 lines 17, 33-34).

Regarding claim 5, the claim rejection for claim 4 is representative of claim 5. See Date et al., disclosure of a memory controller with cache memory (see page 7 lines 8-9).

Regarding claim 7, the claim rejection for claim 3 is representative of claim 7. See Date et al., disclosure of a crossbar switch (see page 14 lines 14-16).

Claims 6 & 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Toujima et al. (US Patent No. 5,999,654) & Date et al. (European Patent No. 0,893,766) & Zimmerman et al. (US Patent No. 5,490,237).

Regarding claim 6, Toujima et al., & Date et al., disclose an apparatus according to claim 4, but do not disclose control of the I/O transfer rate. However, Zimmeran et al., discloses an apparatus wherein said transfer control means discriminates an amount of image data stored in said image memory, and when said image data amount reaches an amount by which said image output apparatus can output an image at a predetermined speed irrespective of a difference of processing speeds of said image input apparatus and said image output apparatus, said image data is transferred from

said image memory to said image output apparatus through said switching control means (see column 5 lines 39-48, I/O buffer thresholds are set in accordance with known apparatus speed).

Accordingly, it would have been obvious to one skilled in the art at the time of the invention to have used the enabling of a predetermined data transfer rate as disclosed by Zimmerman et al., because it assures a printer will complete printing of an image without preventing a halt in operation of the apparatuses (column 2, lines 46-50).

Claim 11 recites identical features as claim 6 except claim 11 is a method claim. Thus, arguments similar to that presented above for claim 6 are equally applicable to claim 11.

Claims 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Toujima et al. (US Patent No. 5,999,654) & Date et al. (European Patent No. 0,893,766) & Ohki (US Patent No. 5,757965).

Regarding claim 12. Date et al., discloses an image processing apparatus comprising: at least four buses (see page 7 lines 10-11), with one bus connected to an image memory for storing image data (fig 4, MC bus), another bus connected to a CPU (fig 4, P bus), and yet another to which an image input apparatus and an image output apparatus are connected (fig 4, IO bus 405); In addition to the multiple buses, Date et al., discloses a bus bridge (fig 4, system bus bridge 402) for forming data transfer channels between the different buses in response to a request from a bus master on one of at least said four buses, wherein said bus bridge simultaneously forms two or more data transfer channels (see page 7 lines 5-12); and arbitrating means (IO bus

arbitrator 407) for arbitrating a plurality of requests from the bus master on one of at least said four buses when said data transfer channel is formed by said bus bridge.

However, although Date et al., discloses a CPU connected to the bus, they do not disclose two coding/encoding means and a bus connected to each of the coding/decoding means.

Toujima et al., discloses an image processing apparatus comprising a first bus (fig 4, bus 63) that is connected to a coding/decoding unit (fig 4, encoder 51). Ohki discloses a main control unit 3 in an image processing apparatus that comprises a CPU to control the compression of image data for output to an output device (column 3 lines 8-15).

Accordingly, it would have been obvious to one skilled in the art at the time of the invention to have used the main control unit of Ohki in replacement of the CPU of Date et al., because it allows for coding of image data. Furthermore, adding the bus-connected encoder disclosed by Toujima et al., to the parallel processing system of Date et al., & Ohki, allows for multiple coding elements which result in more coding speed, decreasing the amount of time it takes to process the image data in the Data et al., & Ohki apparatus.

Regarding claim 13, the rejection of claim 12 is representative of claim 13. See Ohki disclosure of a main control unit comprising a CPU that controls the whole image processing apparatus (column 3 lines 8-15).

Regarding claim 14, the rejection of claim 13 is representative of claim 14. See Ohki disclosure of the first coding/decoding means executes a coding/decoding process

of the image data by a CPU for managing a whole control of said image processing apparatus (column 3 lines 8-15).

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kyle Pendergrass whose telephone number is (703) 306-3445. The examiner can normally be reached on Monday-Friday 8:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiners supervisor, David K. Moore can be reached on (703) 308-7452. The fax phone number for the organization where this application or proceeding is assigned in (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application of proceeding should be directed to the receptionist whose telephone number is (703) 305-9700.

DAVID MOORE
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